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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,529	01/20/2004	Thomas Brune	PD030009	4221

24498 7590 02/02/2006

THOMSON LICENSING INC.
PATENT OPERATIONS
PO BOX 5312
PRINCETON, NJ 08543-5312

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,529	BRUNE ET AL.	
	Examiner	Art Unit	
	Trisha Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05-28-04,01-20-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are presented for examination.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishida et al. (hereinafter Ishida).

As to independent claim 1, Ishida teaches a method for operating a network of interface nodes (nodes A, B, C, etc., e.g. Figs 1-3, and also Figs. 5-6 for protocol

configuration), in particular IEEE 1394 interface nodes, in which interface nodes are connected via a data bus (bus connecting the nodes) (col. 4 lines 31-51), with at least one of the interface nodes in each case receiving self-ID information from others of the interface nodes after a reset operation on the data bus (bus reset), and with each self-ID information item comprising self-ID data, wherein joint information with joint header data and joint ID data is formed in the at least one of the interface nodes (joint header is formed and joint self-ID data is formed, Figs. 13B, 14, 15 and col. 10 lines 3-39) for the self-ID information which has been received by the other interface nodes, and is stored in a memory device (RAM) in the at least one interface node (col. 10 lines 3-39).

As to independent claim 6, Ishida teaches an interface device (e.g. node interface configuration in Figs. 5-6), in particular an IEEE 1394 interface, which is coupled to a data bus (bus connecting the nodes) (Figs. 1-3 and col. 4 lines 31-51) having: transmission means (e.g. Packet Transmitter in Link Layer, Fig. 5 and col. 7 lines 8-18) for transmitting self-ID information to other interface devices in a network of interface devices; receiving means (e.g. Packet Receiver in Link Layer, Fig. 5) for reception of respective self-ID information from the other interface devices in the network of interface devices after a reset operation on the data bus, with the respective self-ID information comprising self-ID data (self-ID, col. 10 lines 3-38); processing means (e.g. link core 20 and associate circuitry, col. 11 lines 50 to col. 12 line 36) for forming joint information with joint header data and joint ID data on the basis of the self-ID information which is received from the other interface devices; and writing means (e.g. packet division circuit

180 and associated circuitry, col. 12 lines 30-36) for writing the joint information to a memory device (RAM).

As to claim 2, Ishida further teaches the self-ID data for the respective self-ID information comprises a first data word (first quadlet – self-ID) and a second data word (second quadlet – parity information) with the second data word being the complement of the first data word, wherein the second data word is processed in the at least one of the interface nodes in a present operating mode for error checking of the first data word, and wherein the first data word is in each case transferred to the joint ID data, forming the joint information, when no error is found during the checking of the second data word (col. 9 lines 36-42 and col. 10 lines 39-63).

As to claim 3, Ishida further teaches once the process of writing the joint information to the memory device (RAM) has been completed, information about the completion of the process of writing the joint information is transmitted to a driver program (e.g. application layer such as printer driver) for the at least one of the interface nodes, in order to release the joint information for processing with the aid of the driver program (col. 7 lines 45-53, col. 8 lines 45-54, and col. 9 lines 43-50, also note that in IEEE 1394 protocol, transfers may resume as soon as the self-identify process that follows a bus reset has completed).

As to claims 4 and 8, Ishida further teaches the formation of the joint information and/or the writing of the joint information to the memory device is terminated when the at least one of the interface nodes receives information about a further reset operation on the data bus during the formation of the joint information and/or the writing of the joint

information to the memory device (once bus reset occurs, all information relating the connection topology is cleared, col. 4 lines 43-51, and once bus reset is detected, packet shaping is performed, col. 13 lines 20-31).

As to claim 5, Ishida further teaches older joint information is overwritten when the joint information is written to the memory device (RAM), this older joint information being the joint information which was written at least partially to the memory device before the process of writing the joint information (once bus reset occurs, all information relating the connection topology is cleared, col. 4 lines 43-51, and once bus reset is detected, packet shaping is performed and stored in the RAM are wherein the RAM is set with boundaries that divide up the area between the header area and the data area, col. 13 lines 20-31 and col. 15 lines 25-31).

As to claim 7, Ishida further teaches the self-ID data in the respective self-ID information comprises a first data word (first quadlet – self-ID) and a second data word (second quadlet – parity information), with the second data word being the complement of the first data word, and wherein the processing means have associated test means (packet diagnosis circuit 142) in order to use the second data word in a continuous operating mode for error checking of the first data word (packet diagnosis circuit 142 checks the second data work for error, col. 13 lines 61-67).

As to claim 9, Ishida further teaches the interface device distinguished by interruption means (e.g. bus monitor circuit 130, col. 13 lines 6-19) in order to interrupt the formation of the joint information and/or the writing of the joint information to the memory device when information about a further reset operation on the data bus is

received during the formation of the joint information with the aid of the processing means (once bus reset occurs, all information relating the connection topology is cleared, col. 4 lines 43-51, and once bus reset is detected, packet shaping is performed, col. 13 lines 20-31).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses IEEE 1394 bus protocol and/or reset operation:

US Patent 6,978,334 Hiratsuka

US Patent 6,978,327 Ishida et al.

"IEEE Standard for a High Performance Serial Bus", IEEE Std 1394-1995, pages 235-236.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu
Examiner
Art Unit 2112

uv

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
1/30/06